ABSTRACT

Data is transferred on a field programmable gate array (FPGA) by (1) retrieving a first set of data from a first block RAM column of a configuration memory of the FPGA, (2) storing the first set of data retrieved from the first block RAM column in a frame data output register, (3) transferring the first set of data from the frame data output register directly to a frame data input register through a configuration bus of the FPGA, and (4) transferring the first set of data from the frame data input register to a second block RAM column of the configuration memory. The configuration bus is wide (e.g., 32-bits), thereby resulting in a high data transfer bandwidth.